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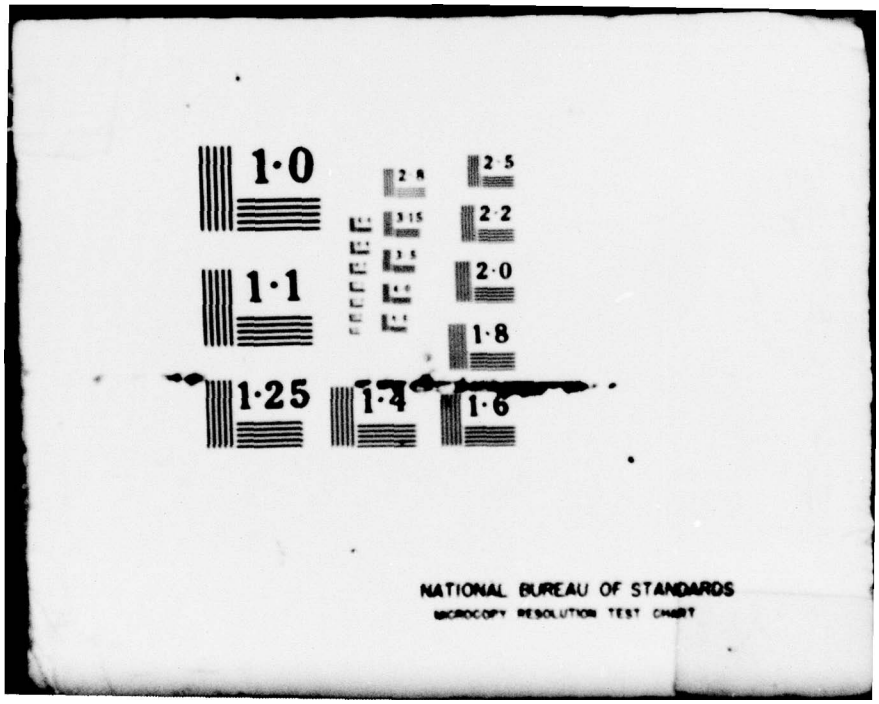
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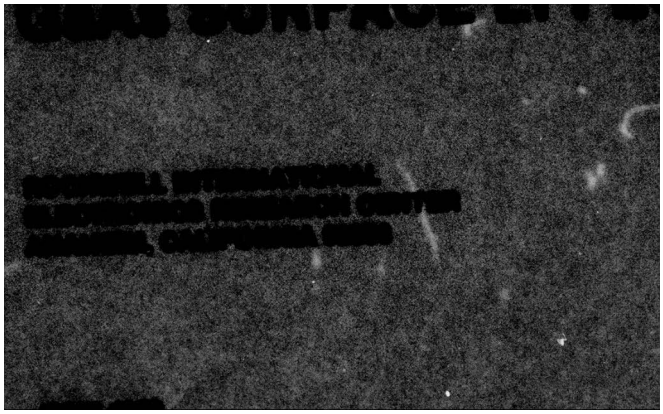

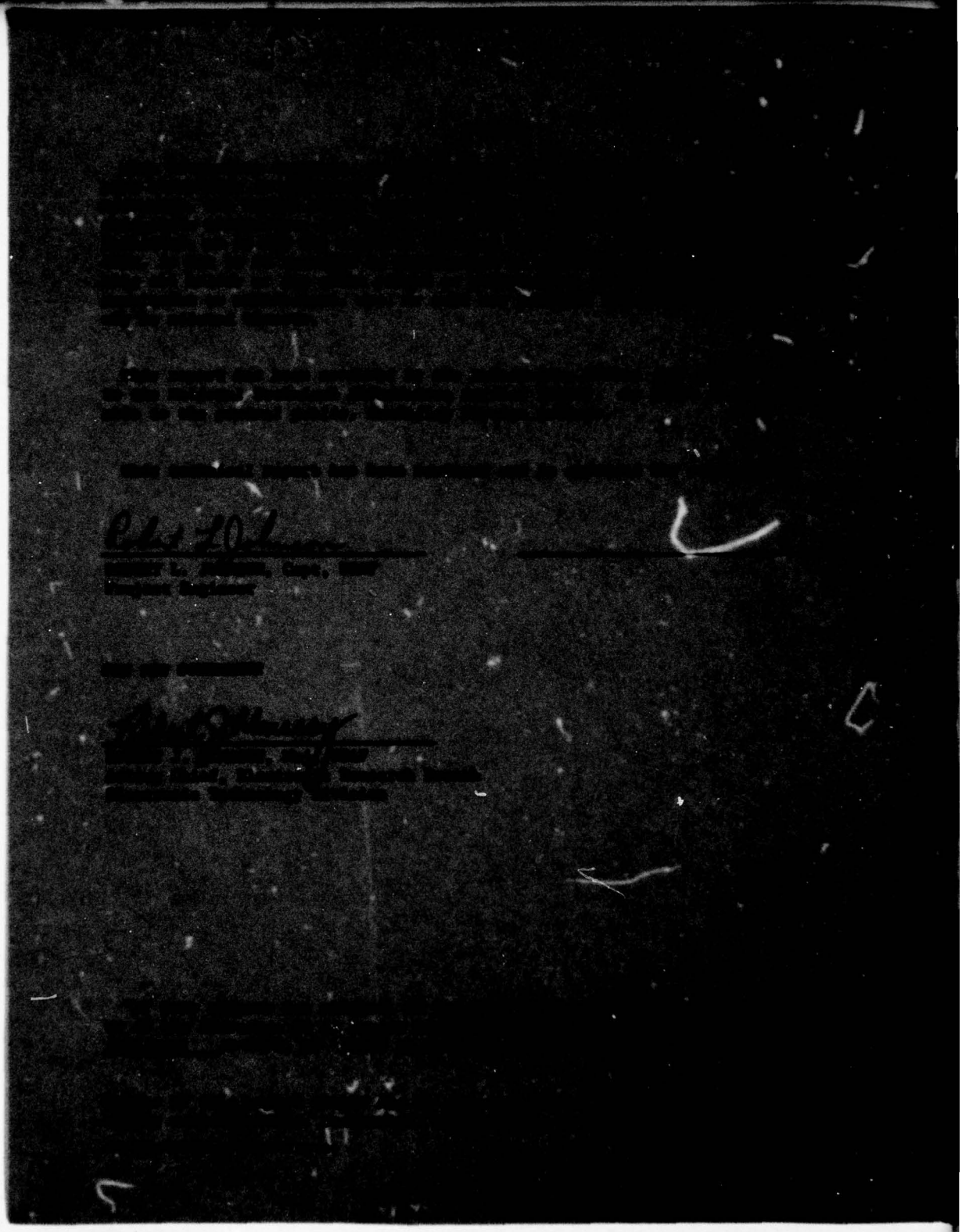

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the results of the first six months of a program to investigate the passivation of GaAs surfaces using a native insulator. Ion implantation of phosphorus and subsequent oxidation of the surface was used to form the insulator.

Post-implant annealing indicates that CVD SiO_2 has somewhat better encapsulating properties than sputtered Si_3N_4. It was found that high-dose phosphorus implantation significantly reduces

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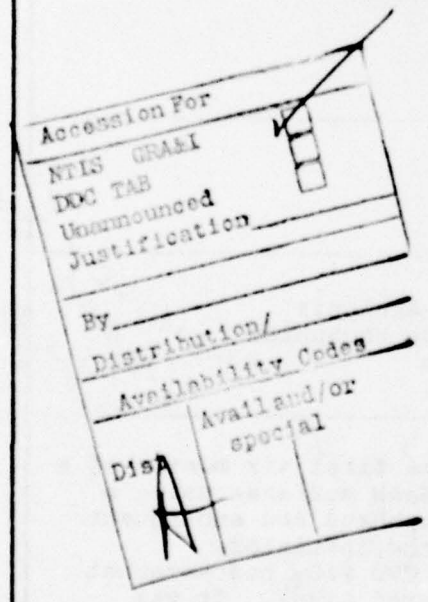
decomposition of the semiconductor surface under the SiO_2 encapsulant during high-temperature annealing.

Annealed and unannealed surfaces were oxidized at 600°C in dry O_2. Results of the oxidations demonstrated that the highest quality films are grown on unannealed surfaces which received doses of 1 to 2 x 10^{16} phosphorus ions/cm^2 implanted at energies of 30 to 60 keV.

Ion microprobe analysis of the implant profiles indicate that phosphorus diffusion is not significant during either high-temperature annealing or oxidation. Elemental depth profiles of oxide layers indicate phosphorus incorporation into the film in the region from the peak of the implant to the interface with the semiconductor. A lack of arsenic and phosphorus at the oxide surface indicates that this region may be composed primarily of Ga_2O_3.



FOREWORD

The research reported herein was supported by the U. S. Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio 45433, under Contract No. F33615-78-C-1591. This research was conducted at Rockwell International Electronics Research Center, Anaheim, California, 92803, during the period 1 July to 31 December 1978. G. Kinoshita was the Program Manager, and G. J. Kuhlmann was the Project Scientist. Capt. Robert Johnson was the Air Force Project Engineer and Technical Contract Monitor.

The primary objective of this three-year research program is to investigate the passivation of gallium arsenide (GaAs) surfaces and the application of dielectric thin-film overlayers in metal-insulator-semiconductor field-effect transistors (MISFETs). The program is divided into three phases: Material and Native Oxide Development, Passivation Development, and MISFET Development. This report describes work performed relative to the initial phase of the Material and Native Oxide Development task.

The author is indebted to the following people for their contributions to this program: R. Drouet--wafer processing and oxidation; F. A. Rhoads and J. Cooper--ion implantation; R. E. Johnson--electron diffraction; and N. Marquez, Aerospace Corporation--ion microprove measurements. He would also like to thank his former colleagues, Dr. D. H. Phillips of Lockheed Corporation and Dr. R. Pancholy of Hughes Aircraft Company for contributions at the inception of the program.

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SECTION I

INTRODUCTION

This report describes work performed from July 1, 1978 to January 1, 1979 on AFSC Contract No. F33615-78-C-1591, "GaAs Surface Effects." The primary objective of this three-year research program is to investigate the passivation of gallium arsenide (GaAs) surfaces and the application of dielectric thin film overlayers in metal-insulator-semiconductor field-effect transistors (MISFETs).

Surface passivation insulators are used as barriers to deleterious environmental influences to improve the stability and performance of semiconductor devices. Thermally grown SiO_2 has resulted in the highest quality passivation layers in the silicon technology; however, limited research has been performed to study the effectiveness of thermally grown native insulators as passivation layers for III-V compound semiconductors. Although many device applications require an extremely low dielectric/semiconductor interface state density, all semiconductor devices benefit from surface passivation insulators which act as a barrier to contamination and which decrease junction leakage currents.

Several different methods have been investigated for forming passivation dielectrics on GaAs. These include thermal oxidation, deposited insulators, and both liquid and plasma anodization. Most of these insulators have proved to be inadequate for many device applications because of excessive dielectric leakage, large interface state densities, and/or charge trapping in the oxide.

Oxides grown using the anodic and plasma techniques generally require post-oxidation annealing treatments at elevated temperatures for stabilization. The major difficulty associated with thermal oxidation is related to the high equilibrium vapor pressure of arsenic above about 450°C, which results in arsenic loss and non-stoichiometry at the oxide-semiconductor interface. Because of this loss, thermal oxidation of GaAs results primarily in crystalline gallium oxide (β-Ga_2O_3), which has not proven to have suitable dielectric and passivation characteristics.

Previous studies of the thermal oxidation of the alloy $GaAs_{1-x}P_x$ (References 1-5) have indicated the possible importance of phosphorus, through the presence of stable gallium phosphate ($GaPO_4$) in forming a higher quality dielectric than is attainable by simply oxidizing GaAs. Gallium arsenide phosphide ($GaAs_{1-x}P_x$), unfortunately, is not the optimum choice for many of the device applications suited for GaAs. This situation occurs because the bandgap energy increases and electron mobility decreases as the phosphorus mole fraction, x, increases. If, however, only the semiconductor surface region is modified by a suitable species such as phosphorus, and subsequently oxidized, a native layer may result which is composed primarily of $GaPO_4$ and has good passivating properties over a GaAs substrate.

The initial phase of this program (Material and Native Oxide Development) will concentrate on investigating the use of ion-implantation techniques to modify the GaAs surface with phosphorus for subsequent oxidation and formation of a device quality dielectric.

The second phase of the program (Passivation Development) will investigate the applicability of the dielectric developed during the initial phase to device passivation applications. Finally, the third phase effort (MISFET Development) will involve investigating the use of the developed passivating insulator as an active gate dielectric in simple discrete GaAs MISFET device structures, as well as simple logic circuits.

This report describes the work performed relative to the initial phase of the Material and Native Oxide Development task. Section II presents a brief description of the ion implantation/oxidation approach for forming GaAs surface passivation layers, and discusses some of the aspects of this approach which are crucial in determining its applicability to the development of device quality insulators. Section III of the report describes the experimental procedures used and presents the results achieved to date. An assessment of these results, and plans for the next reporting period, are given in Section IV.

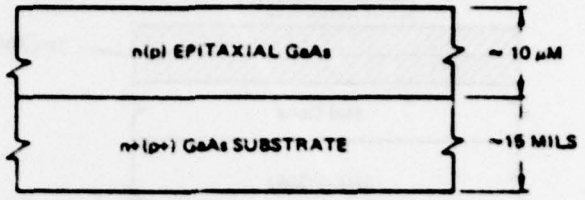
SECTION II

NATIVE SURFACE PASSIVATION LAYER FORMATION ON GaAs USING ION-IMPLANTATION AND SUBSEQUENT OXIDATION

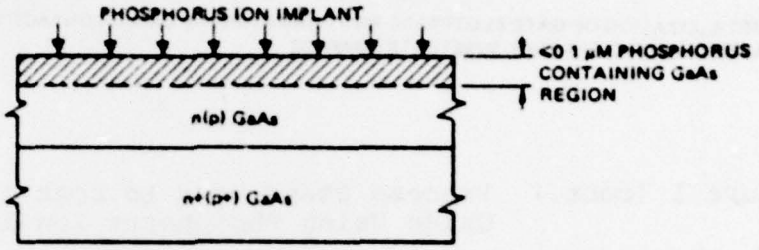
This section briefly describes the technical approach selected for investigation during this initial program phase, as well as the critical areas which must be evaluated in order to assess the feasibility of the approach. Experimental results are presented in Section III.

Basic Approach

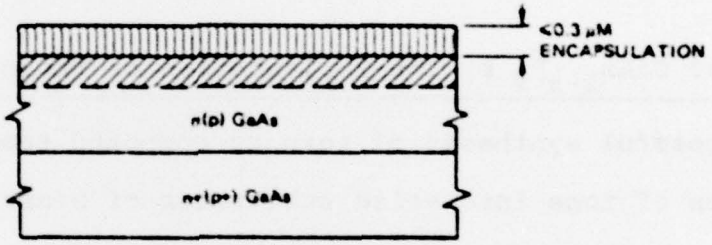
Studies of the thermal oxidation of $GaAs_{1-x}P_x$ (References 1, 2 and 5) have resulted in the formation of a native dielectric which may possess some properties suitable for MOS applications. In order to utilize the desirable properties of a dielectric formed in such a manner and still retain the high electron mobility of GaAs, it is desired to form a thin (~0.05-0.10 μm) phosphorus-containing surface layer which in turn can be oxidized to form the insulator. One method to form such a layer is through the introduction of phosphorus by ion implantation (Figure 1). This approach not only provides control over ion-dose (i.e., the phosphorus mole fraction, x, in $GaAs_{1-x}P_x$) and ion-energy (thickness of the surface $GaAs_{1-x}P_x$ layer), but is compatible with present semiconductor device manufacturing techniques.



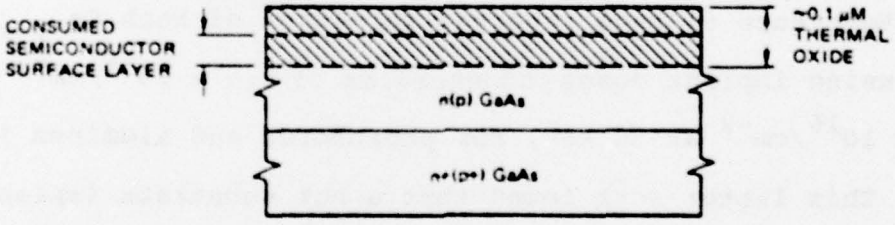
(a) STARTING MATERIAL IS LIGHTLY DOPED n- OR p-EPITAXIAL GaAs ON n+ OR p+ GaAs SUBSTRATE



(b) PHOSPHORUS ION IMPLANTATION OF SELECTED ION ENERGY AND DOSE

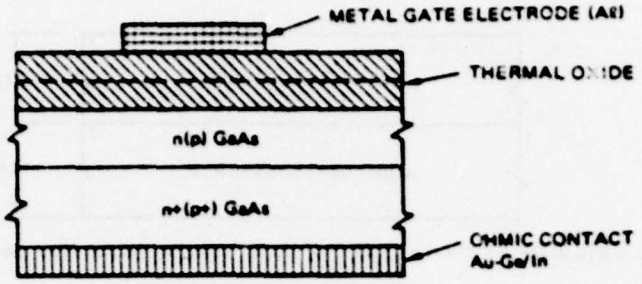


(c) OPTIONAL DEPOSITION OF ENCAPSULANT AND THERMAL ANNEALING IN H_2 OR VACUUM (CAPLESS) ANNEAL. SUBSEQUENT REMOVAL OF ENCAPSULANT



(d) THERMAL OXIDATION OF PHOSPHORUS CONTAINING SURFACE LAYER

Figure 1. Process Steps Used to Form a Thermal Oxide Using Phosphorus Ion Implantation



(e) METALLIZATION OF GATE ELECTRODE AND FORMATION OF OHMIC CONTACT TO n+ (p+) SUBSTRATE AFTER LAPPING THE BACK SUBSTRATE SURFACE

Figure 1 (cont.) Process Steps Used to Form a Thermal Oxide Using Phosphorus Ion-Implantation

Synthesis of $GaAs_{1-x}P_x$ by Ion-Implantation of Phosphorus into GaAs

Successful synthesis of ternary compound semiconductors by implantation of ions into solid substrates of binary compounds has been reported (References 6-9). Most of this work has involved the implantation of either aluminum or phosphorus into gallium arsenide. Belyi, et al (Reference 6) have reported formation of both $Ga_{1-x}Al_xAs$ and $GaAs_{1-x}P_x$ using implant doses and energies of $3.5 \times 10^{16}/cm^{-2}$ at 20 keV and $5 \times 10^{16}/cm^{-2}$ at 30 keV, for phosphorus and aluminum ions, respectively. This latter work found that a hot substrate implant (420°C-500°C) was effective in synthesizing a relative defect-free ternary compound, as determined by luminescence spectra. Some of the aspects of the synthesis of $GaAs_{1-x}P_x$ by implantation, and their relation to this program, are discussed below.

Phosphorus Implantation Dose and Energy Considerations

The previous thermal oxidation work on $GaAs_{1-x}P_x$ (References 1, 2, 4, 5) and GaP (References 10 and 11) has indicated that the presence of phosphorus in the starting semiconductor results in the formation of gallium phosphate ($GaPO_4$) as one of the primary oxidation products. A comparison of the results of compositional depth profiles of the thermal oxides grown on several different binary compound semiconductors (Reference 11) indicated that only in oxides on gallium phosphide (GaP) are the elements perfectly oxidized. In the case of the present ion implantation approach, it is not known whether a high phosphorus mole fraction will be required to achieve a dielectric of sufficiently high quality. It is also not known whether all of the implanted species must be incorporated into the lattice before the same oxidation kinetics and reaction products result as with the previous single-crystal $GaAs_{1-x}P_x$ experiments. With implanted phosphorus ions uniformly distributed in the surface layer and fully incorporated into the lattice structure to form single-crystal $GaAs_{1-x}P_x$, oxidation kinetics and products are expected to be similar to those of the previous work. The phosphorus concentration will not be uniformly distributed through the surface region using a single implant; however, a range of phosphorus percentage (e.g., $x = 0.2$, 0.5, etc.) can be specified, which may result in oxides similar to those previously grown on single-crystal $GaAs_{1-x}P_x$.

Although it may be desirable to keep the phosphorus concentration in the surface region high to result in a maximum of gallium

phosphate in the insulator, there are two reasons for keeping the phosphorus implant dose as low as possible. The first reason is that the electron mobility in $GaAs_{1-x}P_x$ decreases as the phosphorus mole fraction is increased from $x = 0$ to $x = 1.0$, with a sharp transition occurring at approximately $x = 0.4$ (Reference 12). If the entire phosphorus-containing layer is consumed during the oxidation step, then this problem will be alleviated because the semiconductor beneath the insulator will be gallium arsenide (i.e., $x = 0$). The second reason for using a lower phosphorus implant dose, if possible, is that any implantation-induced crystal lattice damage, if present, would be expected to be reduced. Based on these considerations, the initial investigations have been aimed toward formation of a surface layer which contains a phosphorus mole fraction range of $0 \leq x \leq 0.4$.

To calculate in a simplified manner the depth and the peak concentration of an implanted gaussian distribution (Figure 2), the projected range, R_p, of the implanted ions and the deviation about the mean, ΔR_p, are required. The projected range statistics for phosphorus in gallium arsenide are not tabulated, and approximations must be used. It has been observed that, with an atomic density correction, the results for a binary compound are indistinguishable from those of a target element whose atomic number is the average of those of the elements in the compound (Reference 13). Because the range statistics are directly proportional to atomic density, only a simple scaling factor is required in the conversion. In the present case, the tabulated range statistics for phosphorus

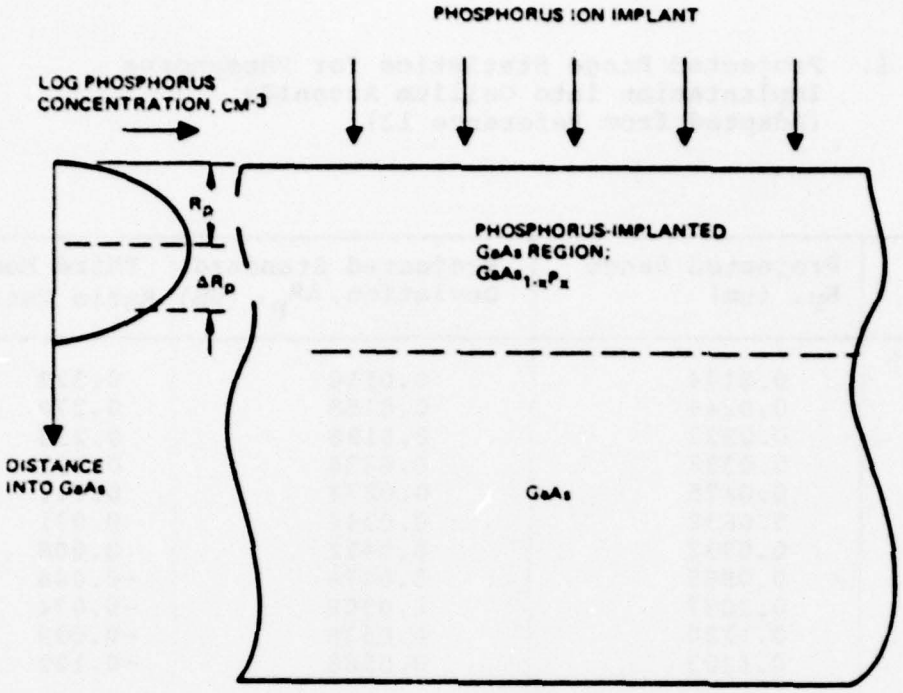


Figure 2. Phosphorus Implant Profile

in germanium (Z = 32) will be used to approximate those for phosphorus in gallium arsenide [gallium (Z = 31) and arsenic (Z = 33)]. The atomic density of Ge is 4.42×10^{22} atoms/cm^3, and the molecular density of GaAs is 2.21×10^{22} molecules/cm^3 or 4.42×10^{22} atoms/cm^3 (Reference 14). Therefore, no scaling correction is required in this case. Table 1 gives the projected range statistics for selected implant energies of interest in this work.

The thickness of the phosphorus-containing surface region must be accurately controlled, because it is desired that all or most of this layer be consumed during the oxidation step. Therefore, for this investigation the range of the implanted phosphorus ions

Table 1. Projected Range Statistics for Phosphorus Implantation into Gallium Arsenide (Adapted from Reference 13)

Energy (keV)	Projected Range R_p, (μm)	Projected Standard Deviation, ΔR_p, (μm)	Third Moment Ratio Estimate
20	0.0174	0.0116	0.322
30	0.0248	0.0158	0.270
40	0.0322	0.0198	0.223
50	0.0398	0.0236	0.181
60	0.0475	0.0273	0.141
80	0.0632	0.0344	0.071
100	0.0792	0.0412	0.008
120	0.0995	0.0476	-0.048
130	0.1037	0.0508	-0.074
140	0.1120	0.0538	-0.099
150	0.1203	0.0568	-0.122

is chosen to be limited to less than 0.1 μm, which corresponds to an implant energy of less than approximately 130 keV for an uncovered GaAs surface. For surfaces coated with an encapsulation dielectric such as SiO_2 or Si_3N_4, appropriate energy corrections must be made to take into account the thickness of such films.

With the projected range information available, approximations of the required ion implantation dose can be made. As an example, assume a $GaAs_{1-x}P_x$ layer is to be formed with a phosphorus mole fraction of $x = 0.33$. Let it be assumed that all of the implanted phosphorus atoms are completely activated and that the replaced arsenic atoms are lost during high temperature annealing and/or oxidation steps. The molecular density of GaAs is 2.2×10^{22}

molecules/cm^3, and because the number of gallium atoms must remain constant and available for bonding to the implanted phosphorus atoms to form the alloy, the gallium atom density is 2.21×10^{22} atoms/cm^3. If N_{Ga}, N_{As}, and N_P are the atomic densities of gallium, arsenic, and phosphorus, respectively, then

$$N_{Ga} = N_{As} + N_P = 2.21 \times 10^{22} \text{ cm}^{-3}, \tag{1}$$

to form a stoichiometric alloy of $GaAs_{1-x}P_x$. It should be noted again that the originally present arsenic atoms which have been replaced by phosphorus are unaccounted for in this expression.

In the present example of $x = 0.33$, then

$$N_{As} + N_P = (2N_P) + N_P \, , \tag{2}$$

and

$$N_{Ga} = 3N_P \tag{3}$$

or

$$N_P = \frac{N_{Ga}}{3} = 7.35 \times 10^{21} \text{ atoms/cm}^3 \tag{4}$$

The implanted phosphorus ion dose required to produce 7.35×10^{21} atoms/cm^3 can be calculated assuming a gaussian distribution and using the simplified expression (Reference 13)

$$N_P \approx \frac{N_I}{2.5 \, \Delta R_P} \tag{5}$$

where N_P is the peak concentration/cm^3 in the implanted region, R_P is the projected standard deviation given in Table 1, and N_I is the implanted dose in ions/cm^2. Therefore, if an energy of 60 keV is chosen ($R_P \sim 475$Å), then the required implant dose is approximately 5.02×10^{16} ions/cm^2.

Table 2 gives the implant dose and energy values required to achieve several different phosphorus mole fractions of interest in the region of the implant peak. These values are for samples in which ions are implanted directly into the surface (i.e., not through an encapsulant.)

Table 2. Phosphorus Implant Parameter Values of Interest

Peak Phosphorus Mole Fraction x	Implant Energy (keV)	Implant Dose (cm^{-2})	Approx. Implant Layer Thickness (Å) ($R_p + \Delta R_p$)
0.10	30	8.73×10^{15}	400
	60	1.51×10^{16}	750
	100	2.28×10^{16}	1200
0.20	30	1.75×10^{16}	400
	60	3.02×10^{16}	750
	100	4.56×10^{16}	1200
0.30	30	2.62×10^{16}	400
	60	4.53×10^{16}	750
	100	6.84×10^{16}	1200
0.40	30	3.49×10^{16}	400
	60	6.04×10^{16}	750
	100	9.12×10^{16}	1200
0.50	30	4.37×10^{16}	400

As in silicon device technology multiple implants of various energies can be used to tailor a relatively uniform phosphorus concentration throughout the surface layer. However, due to the long times required to achieve some of the higher implant doses, initial experiments have investigated single implants.

Additional Considerations in Forming $GaAs_{1-x}P_x$ Layers

Phosphorus Implant Damage--The high-dose low-energy phosphorus implants are expected to result in the formation of an amorphous region near the semiconductor surface. Few experimental results are available for phosphorus implantation into GaAs. However, several other species have been implanted into GaAs, and results from these experiments can be used to anticipate the behavior of the phosphorus implant. A post-implant high-temperature annealing treatment is generally required to electrically activate dopant species, such as Se, S, or Be, and to remove implant-induced crystal lattice damage. This annealing step is usually performed using an insulator encapsulant to avoid thermal decomposition of the GaAs surface. [Problems associated with this procedure are described later.]

The present situation is somewhat different because electrically active species are not being intentionally implanted. However, to provide a crystalline $GaAs_{1-x}P_x$ surface layer whose structure is similar to that used in previous oxidation studies (References 1-5), it is expected that a post-implant anneal or hot substrate implant will be required. It is not known whether restructuring the semiconductor is even a necessary condition for forming a good quality insulator. The initial experimental results of this program, described later, indicate that recrystallization may not be required.

A recent publication (Reference 9) discusses the formation of defects created by phosphorus implantation into GaAs at doses of interest in this work. Rutherford backscattering analyses indicate that an amorphous surface layer resulted only for room temperature implants.

However, defect distribution profiles extended deeper (4000Å) into the substrate for implant temperatures up to 400°C. The total defect density decreased as the implantation temperature increased and this behavior was mainly due to a decrease in the surface defect density. The presence of the deeper defect profile tails was attributed to the acceleration of defect diffusion as a result of the irradiation. This assumption was supported by the fact that the defect profile tails were similar for both the hot and room temperature implants. A slightly earlier work (Reference 15) found, using cathodoluminescence, that no defect region existed under the phosphorus-implanted region. However, a defect region was found for the case of aluminum implanted into GaAs and its formation was attributed to excess gallium atoms being forced into the bulk of the crystal. In the case where a volatile (group V) component is replaced, such as for phosphorus implantation, it was stated that the excess gallium required for reaction is probably formed by evaporation of the arsenic.

Because of the discrepancies in these earlier works, it is not known whether the formation of defects is a significant problem, particularly in the present case where it is desired to consume most or all of the implanted region during thermal oxidation. If defect regions extend deeply into the semiconductor, then deep traps or oxide-semiconductor interface states may result and degrade ultimate MOS device performance. The experimental investigation of possible amorphous-layer and defect-region formation, and the effects of both hot substrate implantation and post-implant annealing, is discussed later.

Post-Implant Encapsulation and Annealing--As mentioned earlier, an insulator is usually used to protect the gallium arsenide surface from thermal decomposition, due to arsenic loss, during high-temperature post-implant annealing. The insulator usually used for encapsulation is silicon nitride (Si_3N_4) (References 16-18), although silicon dioxide (SiO_2) (References 19-21) and double layers of nitride/oxide (Reference 22) have also been investigated. In most cases the ions are implanted through the insulating layers and the samples are then annealed. In addition to the use of an encapsulant, several workers (References 23-25) have investigated capless annealing under various conditions.

The post-implant annealing temperature significantly influences the total disorder remaining after ion-implantation, as described earlier. Because of the volatility of arsenic at the annealing temperatures required for crystal restructuring, both the structural quality and adherence properties of the deposited encapsulant are critical for maintaining surface stoichiometry.

Some workers (References 16, 19) have found that deposited SiO_2 is unsuitable for encapsulation because gallium from the substrate tends to diffuse through the oxide. Other workers, however, (Reference 21) have found that SiO_2 is as effective as Si_3N_4 as an encapsulant. Recently (Reference 22) annealing temperatures as high as 1100°C have been achieved using a Si_3N_4/SiO_2 double layer. Although nitride encapsulants are now commonly being used in GaAs device fabrication processes, a wide variety of effects, including adherence problems, cracking and blistering at high annealing temperatures, have been observed. The quality and repeatability of the annealing process

appear to be very sensitive to both the surface preparation prior to encapsulant deposition, and the type of deposition process itself (e.g., plasma or sputtered). Because of the variable results reported in the literature and those obtained thus far in this program, it appears that the encapsulation/annealing process is not fully understood and remains somewhat an art.

Few capless annealing results have been reported, and most of those which have been presented depend on a sealed tube and over-pressure of arsenic to minimize surface decomposition. These techniques do not appear to be suitable for large-scale device production. A recent result (Reference 25) in which uncapped implanted surfaces were in intimate contact with the surface of another GaAs wafer, indicates that there may be some hope for a simplified capless annealing procedure.

Oxidation Considerations

Oxidation Temperature and Time--The upper temperature limit for the growth of acceptable thermal oxides on $GaAs_{0.5}P_{0.5}$ has been established as 700°C (Reference 1). More recent work (Reference 4) has indicated that a lower oxidation temperature reduces arsenic-loss from the oxide and also results in lower dielectric leakage currents. Similar oxidation behavior to that observed previously would be expected in the case of an ion-implanted surface if the phosphorus concentration is uniform and crystallinity is completely restored by annealing. However, the effect on the oxidation behavior of the excess arsenic which must be replaced by the phosphorus is not known. In addition, the effects on the oxidation

behavior of a nonuniform phosphorus concentration with depth, using a single implant, and the possibility of incomplete annealing are unknowns to be evaluated. Some initial results are given in a later section.

Oxide Thickness--The thickness of the grown oxide can be controlled by the ion-implant energy and subsequent high temperature processing steps. From the results of thermal oxidation on bulk $GaAs_{1-x}P_x$ (Reference 26) it is expected that the ratio of the thickness of the semiconductor consumed to that of the oxide grown is approximately 2/3. For example, to grow a 1000Å-thick oxide, the phosphorus-containing surface region must be approximately 700Å thick. This thickness then determines the selection of an ion-implant which has a mean range of approximately 400Å into the GaAs. Therefore, from Table 1, it is seen that an energy of about 50 keV will be required for an implant into a bare GaAs surface.

Redistribution of Implanted Phosphorus--A final possible effect which must be considered is that of redistribution of the implanted phosphorus during both the annealing and oxidation steps. The diffusion of phosphorus in GaAs has been recently investigated (Reference 27). These workers observed a strong concentration-dependent increase in the diffusion coefficient at all temperatures from 800-1100°C, for phosphorus concentrations near $\sim 10^{22}$ atoms/cm^3. This value is in the concentration range of interest for forming $GaAs_{1-x}P_x$. At the lower annealing and oxidation temperatures (500-800°C) used in the present work, however, thermal redistribution is not expected to be a significant problem. The experimental results presented later tend to confirm this.

SECTION III

RESULTS OF ION IMPLANTATION, ANNEALING, AND OXIDATION EXPERIMENTS

This section presents the results of phosphorus ion implantation, post-implant annealing, and thermal oxidation experiments. These results are discussed with respect to those which were expected, and the problems associated with each process step are also described.

Starting Material and Surface Preparation

GaAs Starting Material--The initial ion implantation experiments have been conducted using (100) bulk n-type (Si-doped) GaAs wafers. The donor concentration specified by the manufacturer is 7×10^{17} to 4×10^{18} cm^{-3}. The donor concentration determined from $1/C^2$ vs. reverse bias voltage plots of Schottky diodes were in the range 1 to 2×10^{18} cm^{-3}. Experiments to deposit thin (2-4 μm) lightly doped epitaxial layers by metal-organic chemical vapor deposition (MO-CVD), which were planned to begin during this period, have been temporarily postponed due to previous equipment commitments. The more heavily doped bulk material is sufficient to provide the required baseline information needed for the implantation and oxidation growth experiments.

Substrate Surface Preparation--To prevent lifting and flaking of the implant encapsulant during high temperature processing, it is desirable that the GaAs surface be as clean and defect-free as possible prior to the encapsulant deposition. To remove organic contaminants the GaAs surfaces underwent a solvent clean in trichloroethane, acetone, and deionized water. This is usually followed by a chemical etch to remove surface damage.

Because thinner (1-3 μm) epitaxial films are planned to be used in the latter phases of this program, this etch step must be well controlled. To determine a solution with the most desirable characteristics for the present application, several component ratio variations of the common GaAs etchant H_2SO_4:H_2O_2(30%):H_2O were investigated. Figure 3 is a plot of the thickness of semiconductor material removed vs. etch time. Many of these solutions left a visible, slightly grainy residual layer on the surface, as illustrated in Figure 4. These surfaces darkened after exposure to air for several days, indicating a surface chemical instability. The use of 'hot' etching solutions (i.e., freshly mixed) reduced this residue, but for many of the component ratios high etch rates (Figure 3) make them impractical for application to thin epitaxial layers.

Because the sulfuric acid-based etch solutions tend to result in somewhat unstabilized surfaces, a basic solution of $20NH_4OH:7H_2O_2:973H_2O$ (Reference 28) was investigated. This solution has an etch rate of approximately 1250Å/min at room temperature, and the resulting surfaces do not exhibit a residual layer. Therefore, this solution has generally been used for the surface polishing.

Many defects were visible in some of the early Monsanto starting material used in the chemical etching experiments. The etch step further delineated these defects, resulting in deep etch pits, as shown in Figure 5. Material received after discussions with the supplier displayed lower defect densities. In general, material

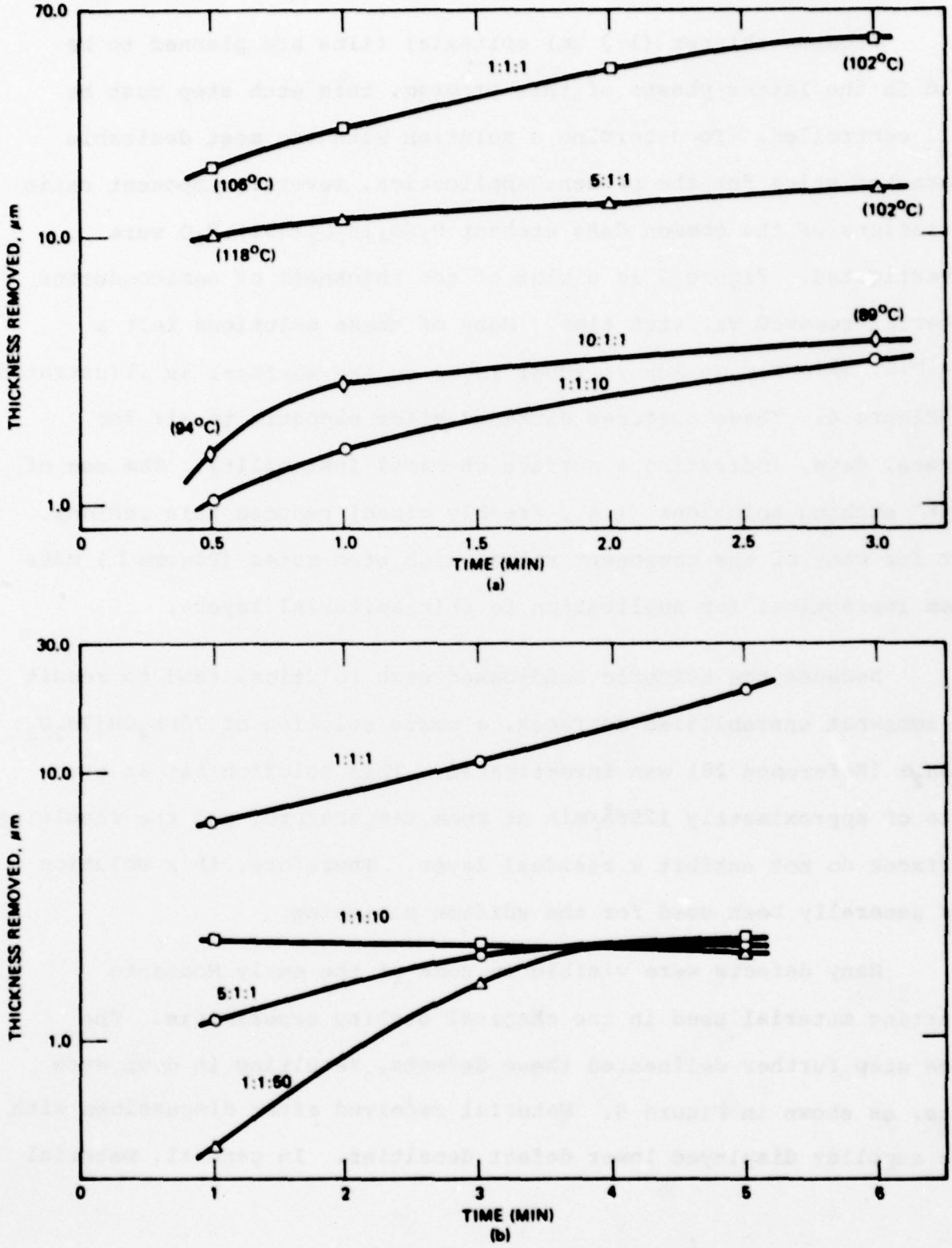


Figure 3. GaAs Removal vs Time for Various Ratios of H_2SO_4:H_2O_2:H_2O.
(a) Fresh Solutions (hot) (b) Room Temperature Solutions

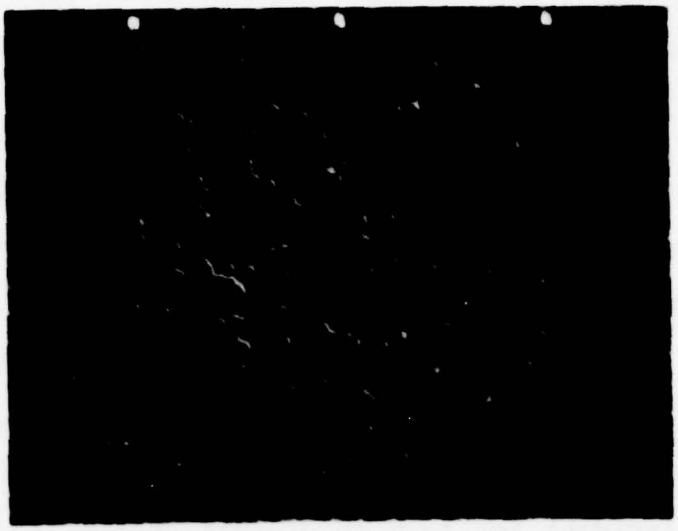


Figure 4. Nomarsky Contrast Photomicrograph of Residual Surface Layer Following Etching in 1:1:10 H_2SO_4:H_2O_2:H_2O (280X)

Figure 5. Etch Pits Resulting from Hot (95°C) 10:1:1 H_2SO_4:H_2O_2:H_2O Surface Cleaning Etch (280X)

obtained from another vendor (Crystal Specialties) has had a relatively low pit density following etching.

Ion Implantation

Implantations were performed using an Extrion Model 200-20 ion implanter. Phosphorus ion currents using this machine ranged from 1 to 3 μA, and implant times were typically 5 to 15 min. to achieve the doses (e.g., $2 \times 10^{16} cm^{-2}$) desired for the annealing experiments. All samples were mounted intimately to the substrate holder using spring clips. The sample holder was then adjusted to an angle of 7° relative to the incident ion beam to prevent channeling along major crystallographic axes. During implantation a small region of each wafer was blocked off to prevent implantation. This procedure allowed a direct comparison of the effects of the various annealing and oxidation steps on both the implanted and unimplanted areas.

Encapsulation and Annealing Experiments

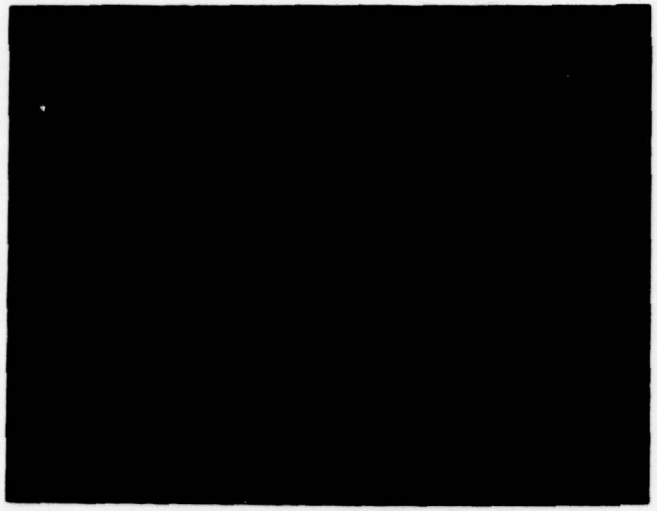
Silicon Nitride--Because of its wide use as an implant/annealing encapsulant, silicon nitride was initially investigated. Low-temperature rf-sputtered nitride films (~3000Å thick) were deposited on GaAs surfaces which had been implanted with 100 keV phosphorus ions to a dose of $1 \times 10^{16} cm^{-2}$. The samples were then annealed in forming gas at various temperatures for a period of one hour. Table 3 summarizes the results of these annealing procedures.

The sputtered nitride begins lifting and flaking, as shown in Figure 6, between 600°C and 700°C. Figure 7(a)-(d) show Nomarski contrast photomicrographs of the surfaces described in Table 3 following a thermal oxidation process at 550°C in dry oxygen for 30 minutes.

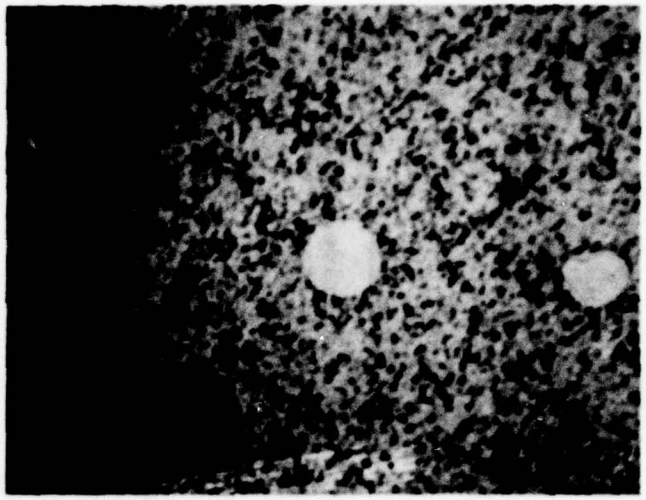
Table 3. Results of Post-Implant Annealing Experiments Using Sputtered Si_3N_4 Encapsulant (t = 3000Å)

Annealing Temp. (°C)	Ambient	Time	Visual Results
400	Forming Gas	1 Hr.	No damage on nitride. No apparent surface damage after nitride removal.
500	Forming Gas	1 Hr.	Spots on nitride surface. No apparent damage after removal.
600	Forming Gas	1 Hr.	Holes appearing in nitride. Damaged regions following removal.
700	Forming Gas	1 Hr.	Nitride flaking and lifting. Damaged regions following removal

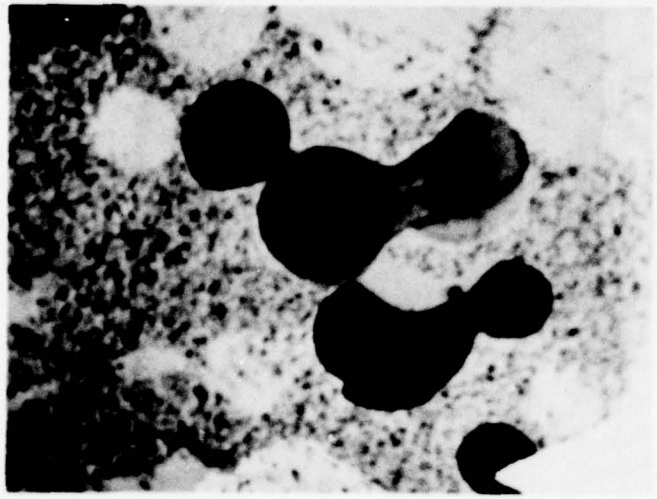
Figure 6. Lifting of Sputtered Nitride Following 600°C, N_2 Anneal for One Hour (97X)



(a) T_{ann} = 400°C



(b) T_{ann} = 500°C



(c) T_{ann} = 600°C

(d) T_{ann} = 700°C

Figure 7. Nomarski Photomicrographs of Oxidized Surfaces Following Implant Anneal at Various Temperatures Using Sputtered Si_3N_4

Oxides grown on surfaces annealed at the two lower temperatures exhibit an extremely heterogeneous appearance [Figure 7(a) and (b)]. At higher annealing temperatures the nitride begins to lift from the surface and the forming gas ambient apparently reacts with the exposed GaAs surface. The subsequent oxidation results in the dark areas shown in Figures 7(c) and (d). The lighter regions of Figure 7(d) correspond to areas of relative uniform oxide growth. This latter result seemed to indicate that higher temperature annealing is required to provide sufficient lattice reordering for oxide growth. The results of subsequent experiments on unannealed surfaces, however, show that this high-temperature anneal is not necessary to obtain uniform oxide growth.

Because of the deleterious annealing properties of the sputtered nitride layers, low-temperature plasma nitride films were also investigated. The annealing results for these samples were essentially the same as those for those with the sputtered layers, with bubbling and lifting occurring at about 600°C.

In the annealing experiments described above, the nitride was deposited directly on the implanted GaAs surface. In silicon technology both SiO_2 and Si_3N_4 films are usually deposited on a thin thermally grown silicon dioxide film to improve adherence and achieve suitable interface properties. To determine if a similar procedure would improve the annealing properties of the nitride, samples were oxidized at 450°C in dry O_2 for 1 hour. This procedure results in a native oxide thickness of approximately 140Å (Reference 29). Following oxidation, 1400Å of silicon nitride was sputtered onto the wafers,

and phosphorus ions were implanted through both layers to a dose of $1 \times 10^{16} cm^{-2}$. The ion energy (190 keV) was chosen such that the concentration peak of the implant lies at or near the semiconductor-native oxide interface. After annealing at 600°C for just 30 minutes, bubbling and lifting of the nitride was observed, as shown in Figure 8.

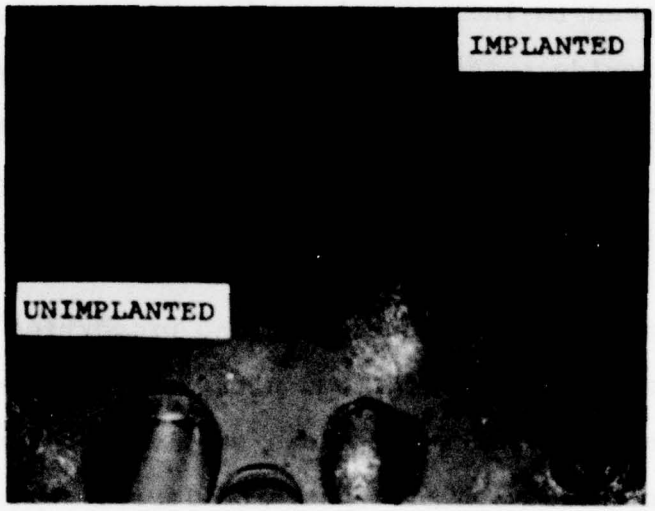


Figure 8. Lifting of Nitride at Implanted-Unimplanted Boundary Region (247X)

The bubbling is more severe in the implanted regions of the wafers. This behavior is in contrast to that observed using silicon dioxide as an encapsulant, where significantly less damage occurred in implanted regions.

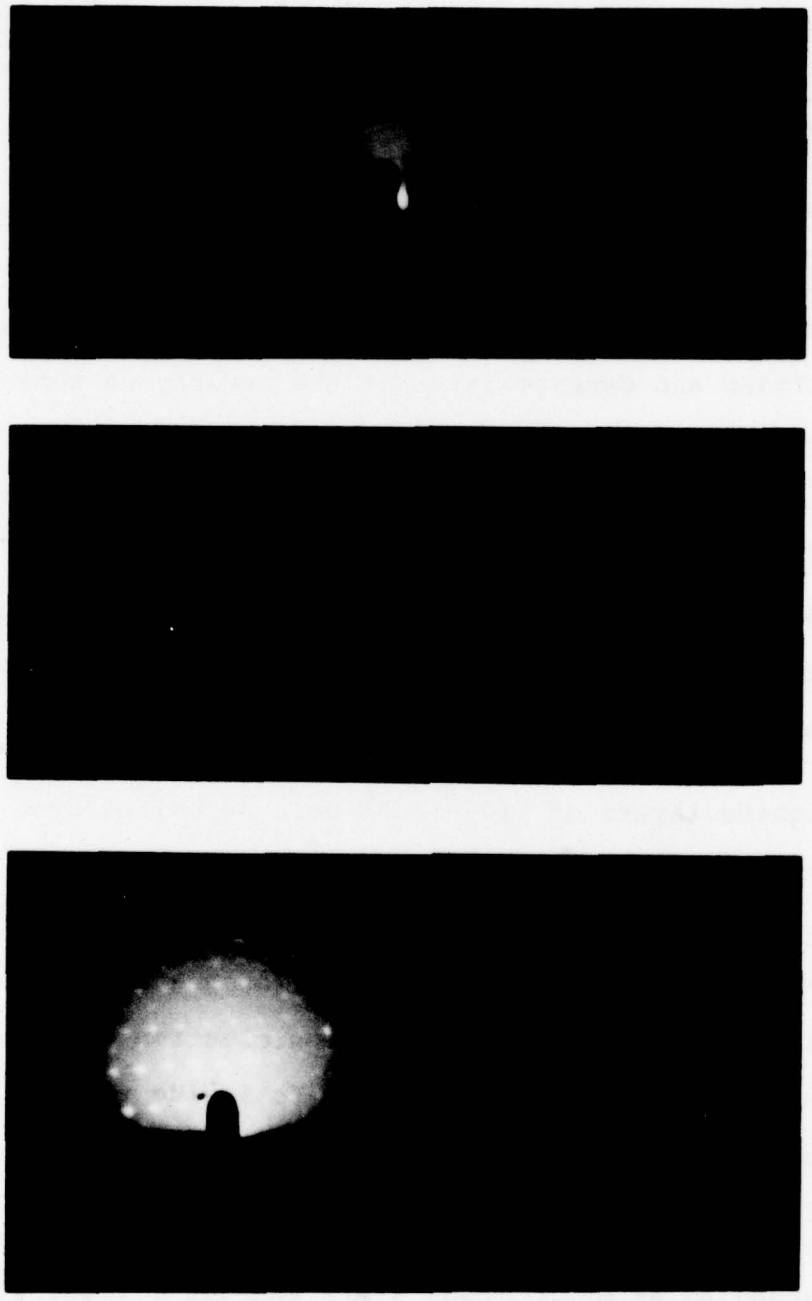
Based on the results obtained thus far in the program, it appears that nitride is not an adequate encapsulant for annealing implantation damage under our experimental conditions. Therefore,

rather than expending an excessive amount of effort in perfecting nitride encapsulation procedures, silicon dioxide was explored as an alternate encapsulant.

Room Temperature Implantation and Annealing Variations Using SiO_2/Native Oxide Encapsulants--The early experiments using silicon dioxide films chemical vapor deposited at 400°C onto bare GaAs surfaces indicated that lifting and decomposition of the underlying semiconductor occurred for annealing temperatures above about 650°C. Use of the thin (~140Å) native oxide underneath the deposited SiO_2 layer, mentioned earlier in connection with silicon nitride films, has significantly improved the annealing characteristics. Therefore, use of these layers was investigated further because they seemed to hold more promise than the other capping layers.

Silicon dioxide layers of 1100-1300Å were deposited over the 140Å-thick native oxide. Phosphorus ions were implanted through the encapsulants at energies ranging from 140 keV to 190 keV. Annealing was then carried out in dry nitrogen for one hour at various temperatures. Figures 9(a)-(c) show reflection electron diffraction (RED) patterns on variously annealed surfaces following removal of the encapsulant. These samples had received an implant dose of $1 \times 10^{16} cm^{-2}$ at an energy of 190 keV.

Surfaces annealed at 650°C (Fig. 9(a)) and 700°C (Fig. 9(b)) show broad faint rings indicative of nonoriented polycrystalline and amorphous material. After a 750°C N_2 anneal for one hour, however, the surface yields an oriented single-crystal type of RED pattern



(a)
650°C

(b)
700°C

(c)
750°C

Figure 9. Reflection Electron Diffraction Patterns of Phosphorus-Implanted ($1x10^{16}cm^{-2}$) GaAs After Annealing for 1 Hour Using SiO_2 Encapsulant.

with Kikuchi lines. These results indicate that restructuring of the crystal is occurring at the surface between 700°C and 750°C.

Samples which had received an implant dose of $3 \times 10^{16} cm^{-2}$ did not display crystalline RED patterns up to an annealing temperature of 750°C, but instead displayed a pattern indicative of a polycrystalline layer over a single-crystal substrate. Therefore, it appears that a higher temperature is required to anneal surfaces implanted to the higher doses.

Attempts to anneal surfaces at 800°C have not been completely successful. Figure 10 shows the severe damage resulting from a 30 minute anneal at 800°C in N_2 using a 1000Å-thick capping layer.

Figure 10. Decomposition of Implanted Surface Following 800°C N_2 Anneal (SiO_2 Encapsulant) (49X)

The decomposition occurs along crystallographic directions, and the films tend to lift around particles or defect regions. The maximum annealing temperature achieved to date (~775°C) is below some that have been reported in the literature. Because the film quality (i.e., the presence of pinholes and inclusions) so critically affects the decomposition observed after annealing, it appears that the maximum annealing temperature can be raised with further improvements in film deposition processes and cleaning procedures. These improvements are continuing.

The sampling depth of the diffracted electron beam used in the RED characterization is~1500Å in gallium arsenide. It should be noted that high-energy RED patterns only give a composite view of the surface region. To detect lower defect densities which may extend deeper into the substrate (Reference 9), a more sensitive technique, such as Rutherford (ion) backscattering, or possibly electroreflectance (Reference 30) should be used. These types of measurements will be performed if arrangements can be made to use this equipment at an external facility.

One significant and somewhat unexpected beneficial result of the high dose implant is its ability to greatly inhibit decomposition of the semiconductor under the encapsulant during high temperature annealing. This effect is illustrated in the photomicrograph of Figure 11 which shows the boundary between an unimplanted region and a region which had been implanted to a dose of $1 \times 10^{16} cm^{-2}$. This sample was annealed at 725°C for 1 hour in N_2, followed by removal of the SiO_2. The damage (gallium flow) areas on the unimplanted side abruptly end at the implant boundary. This behavior contrasts with

that which occurs when using a nitride encapsulant. The reason for this difference may be due to differences in the tensile or compressive stresses which may be occurring at the insulator-semiconductor interface.

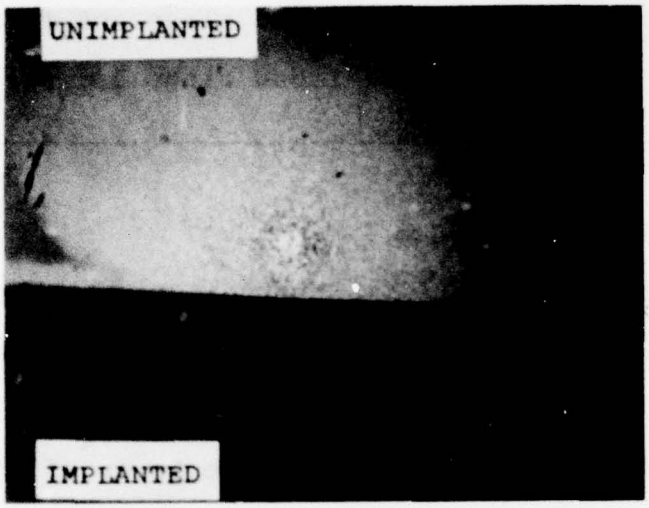


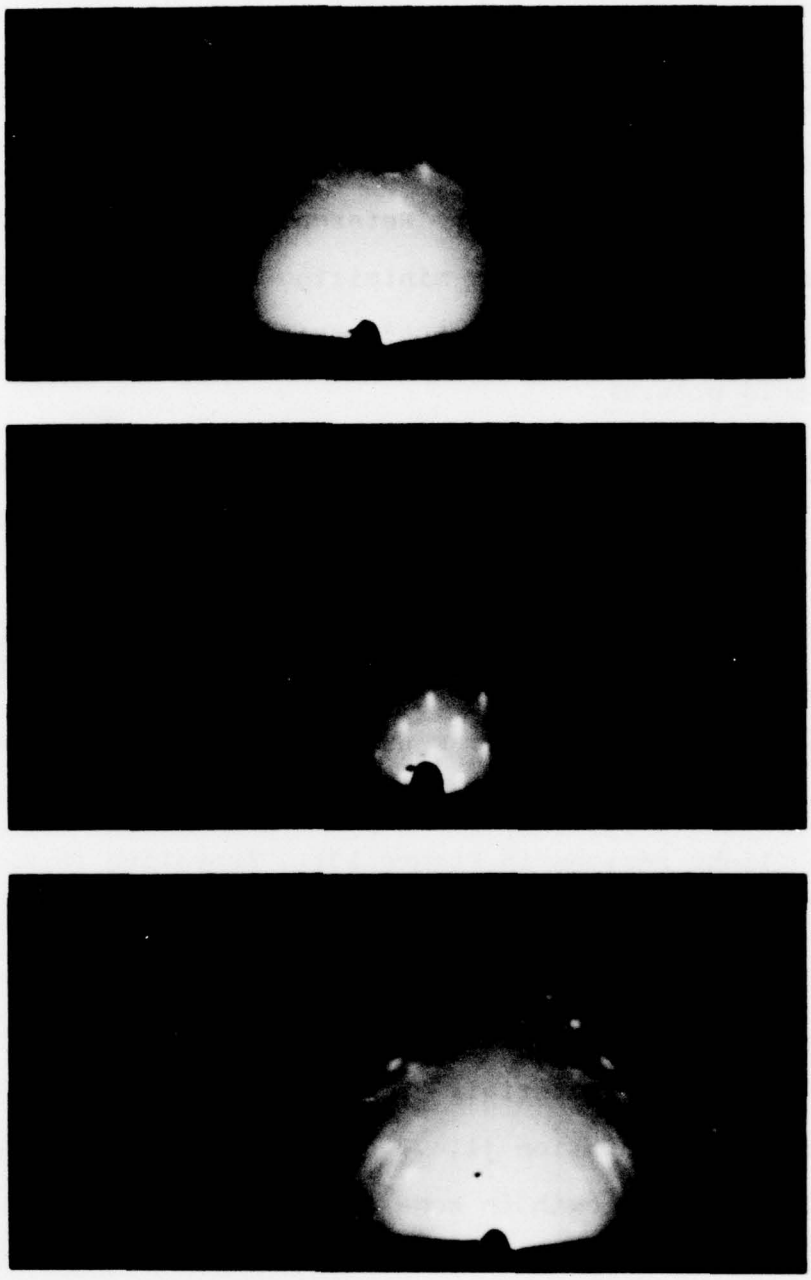
Figure 11. Boundary Between Implanted and Unimplanted Region Following Anneal at 725°C in N_2 Using SiO_2 Encapsulant (247X)

High-Temperature Implantation Using SiO_2 Encapsulant--It has been observed that by elevating the temperature of the GaAs substrate during the implantation, significantly lower lattice damage levels result due to thermal annealing. To examine this effect, implantations were performed on substrates whose temperatures were held at either 300°C or 400°C. Higher temperature implantations could not be achieved because of substrate heater element failure above 400°C.

Table 4. Hot-Substrate Implant Variations
t_{SiO_2}=1100Å, t_{no}=140Å, E_p=140 keV

Implant Dose (cm^{-2})	Implant Temp. (°C)	Reflection Diffraction Pattern
1×10^{16}	300	Broad rings and faint Kikuchi lines
2×10^{16}	300	Broad rings and faint Kikuchi lines
2×10^{16}	400	Broad rings and faint Kikuchi lines

Table 4 lists the 'hot' implant variations attempted thus far. Electron diffraction patterns were made of the surfaces following removal of the capping layers. The results were similar for all variations and indicative of a polycrystalline layer of non-preferred orientation over single-crystal material. Diffraction patterns were also made as a function of depth by chemically removing the surface region. Figure 12(a)-(c) show the patterns for a sample implanted to a dose of $1 \times 10^{16} cm^{-2}$ at 300°C. Although it may not be readily apparent from the photographs, the patterns show increasingly strong Kikuchi lines with depth, indicating that significant damage does not extend deeply into the substrate. The RED patterns for the hot implants are similar to those for room temperature implants which subsequently underwent annaling at 725-750°C. However, oxides grown on the 'hot' samples are generally inferior to those grown on samples implanted at room temperature. This will be discussed further in the next section.



(a)

(b)

(c)

Figure 12. Reflection Electron Diffraction Patterns for Sample Implanted at 300°C through SiO_2 Encapsulant ($1 \times 10^{16} cm^{-2}$, 140 keV)

(a) Surface
(b) 350Å
(c) 800Å

Oxidation of SiO_2-Encapsulated and Annealed Surfaces

Although the early studies on $GaAs_{1-x}P_x$ used an oxidation temperature of 700°C, a later study (Reference 4) indicated that lower temperatures may be attractive for minimizing arsenic loss and improving electrical properties. Therefore, 600°C oxidations have been initially performed for this program.

Annealing Temperature Effects--Following removal of the SiO_2/native oxide layers in buffered hydrofluoric acid, samples were oxidized at 600°C in dry oxygen for various times. Figure 13 shows the surface of a sample (implanted at room temperature to $1 \times 10^{16} cm^{-2}$, 190 keV) which had been annealed at 650°C for one hour in N_2, and oxidized at 600°C for 30 minutes. Nonuniform oxide growth and some gallium flow is observed in several regions with uniform oxide growth in other areas (light regions in Figure 13). Annealing in nitrogen at either 750°C for 30 minutes,or 725°C for one hour, resulted in surfaces which,when oxidized, generally exhibited uniform oxide films, with decomposition only along wafer edges and around defect areas originally present in the material. Regions of wafers which were blocked off during implantation (i.e., gallium arsenide regions) exhibited uniform oxide growth in some areas, but significant decomposition and gallium bubbling in other areas, as shown in Figure 14.

Implant Dose Effects--Oxidation of annealed (725°C)surfaces at 600°C for 2.5 hours in O_2 yielded oxide thicknesses of about 600Å for a dose of $1 \times 10^{16} cm^{-2}$ and 900Å for $3 \times 10^{16} cm^{-2}$, as determined using a Dektak surface profiler. This compares to an oxide thickness of 450-500Å grown over the unimplanted (i.e., GaAs) areas. The previous

Figure 13. Surface Following Annealing at 650°C and Oxidation at 600°C (SiO_2 Encapsulant) (97X)

Figure 14. GaAs Surface After Oxidation at 600°C for 30 Minutes (247X)

oxidation studies of crystalline $GaAs_{1-x}P_x$ (References 2, 4, 5) had shown that the growth rate of oxides decreases for increasing phosphorus content in the semiconductor. However, the behavior in the present case, for implanted surfaces, is opposite to this. The difference in oxidaton kinetics may be due to incomplete annealing of implant-induced lattice damage. Also, as described later, the single phosphorus implant results in a nonuniform concentration of oxide constituents as a function of depth. Thus, oxidation rates would also be expected to be complicated and to vary with depth.

The dose levels investigated thus far ($1\text{-}3 \times 10^{16} cm^{-2}$) result in low phosphorus mole fractions ($0.03 \leq x \leq 0.10$, according to Equ. (5)) after implantation through the capping layer. Although higher phosphorus levels may be desirable to obtain an increased gallium phosphate ($Ga\ PO_4$) content in the oxide layer, initial indications are that optimum growth results may occur at doses less than 3×10^{16} cm^{-2} for the annealed samples. Wafers which had received 3×10^{16} phosphorus ions/cm^2, followed by annealing at 725°C, yielded very grainy surfaces upon oxidation at 600°C, and as shown in Figure 15. Oxides grown on surfaces which had lower implant levels exhibited significantly less graininess, as did oxides grown on unannealed surfaces at the higher dose levels. These effects need to be investigated further.

Hot Implants--Oxides grown on surfaces which had received elevated-temperature implantations were generally nonuniform and of poor quality. Figure 16 shows the oxide grown at 600°C on a sample

Figure 15. Nomarsky Photomicrograph of Oxide Grown on Annealed Implanted Surface (Dose: 3×10^{16} cm^{-2}) (280X)

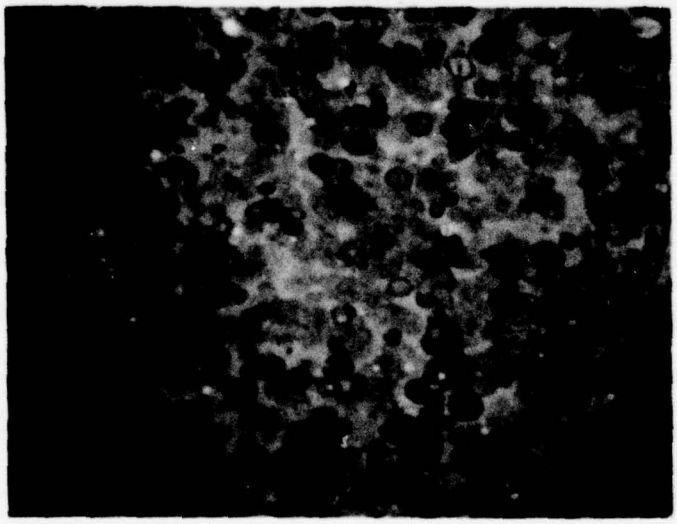


Figure 16. Oxide Grown on Surface Implanted at 400°C (SiO_2 Encapsulant) (247X)

which had a dose of 1×10^{16} ions/cm^2 implanted through a silicon-dioxide encapsulant at 400°C. In this case darker spots of oxide are surrounding particle-like nucleation centers. It is possible that this may be caused by an interaction between the gallium arsenide surface and the silicon dioxide used as an encapsulant. It should be noted, however, that a 750°C anneal following room-temperature implantation did not result in this behavior.

The oxides grown on samples implanted at 300°C show damage similar to that occurring for room temperature implants annealed at lower temperatures (e.g., Figure 13). Encapsulated samples which were annealed at 725°C following the hot implant have exhibited somewhat better quality oxides than those without post-(hot)-implant anneal. These films, however, are still not the quality of those grown on either the room-temperature implanted and high-temperature annealed or the unencapsulated/unannealed samples to be discussed later.

Implant Energy Effects--Some regions of the samples implanted at 190 keV showed decomposition after oxidation. With this implant energy, the projected range of the implanted ions is approximately 700Å into the GaAs (i.e., after passing through the SiO_2 encapsulant). It appears that the phosphorus concentration at the GaAs surface may be too low with the 190 keV implant energy. Therefore, an implant energy of 140 keV was also investigated on samples with the same SiO_2 thickness (~1100Å). With this energy the projected range of the peak is at a depth approximately 300Å from the GaAs surface.

Oxides grown on these surfaces show fewer areas of decomposition than those with the higher energy, indicating that surface phosphorus concentration is critical. The oxidation results on unannealed surfaces also showed that location of the implant peak is important in determining oxide quality. This is described below.

Oxidation of Unannealed Implanted Surfaces

In order to determine if high-temperature annealing using an encapsulant is required to achieve high-quality and uniform oxide growth, samples were oxidized after phosphorus had been implanted directly into the GaAs surfaces. Generally, implant parameter variations have duplicated those used for encapsulated samples.

One concern about low-energy high-dose implantation into a bare GaAs surface is the possible sputtering which may result. To examine if this effect was significant for the phosphorus implants, Dektak surface profile measurements were made across implanted and unimplanted boundary regions. No step could be detected up to the maximum sensitivity ($\lesssim$100Å) of the instrument. Therefore, it appears that sputtering effects are not important for these implant conditions.

Implant Dose Effects--Implant doses ranging from $6 \times 10^{15} cm^{-2}$ to $3 \times 10^{16} cm^{-2}$ have been investigated initially. The implant energy used for these experiments was fixed at 60 keV. Table 5 summarizes the effects of these dose variations. A dose of $6 \times 10^{15} cm^{-2}$ is apparently too low to result in uniform oxide growth, and areas of decomposition are scattered about the surface. Medium-dose implants ($1\text{-}2 \times 10^{16} cm^{-2}$) generally result in uniform oxides with little or

Table 5. Results of Phosphorus Ion Dose Variations for Unannealed Surfaces (60 keV, Rm. Temp. Substrate). Oxidation: 600°C, O_2

Dose (cm^{-2})	Oxidation Time (Hr.)	Approx. Oxide Thickness (Å)	Remarks
6×10^{15}	0.5	400	Decomposition near wafer edge
	1.5	550	Slightly grainy, slight decomp.
	2.5	600	Areas of decomposition
1.8×10^{16}	0.5	400	Uniform, no damage
	1.5	550	Uniform
	2.5	625	Uniform, minimal damage
3×10^{16}	0.5	650	Slightly grainy, scattered white spots
	1.5	800	Uniform, a few small spots
	2.5	900	Same as above

no decomposition apparent. Films grown in this dose regime display only slight structure (graininess) similar to that observed in thermal oxides grown on $GaAs_{1-x}P_x$ at the same temperature. An implant dose of $3 \times 10^{16} cm^{-2}$ yields thicker uniform oxides than the lower doses, but there are a few very small white 'particle-like' spots interspersed in the oxide matrix. These do not appear to be nucleation regions for decomposition, and are being investigated further using higher implant doses ($>3 \times 10^{16} cm^{-2}$).

Implant Energy Effects--The effects of implant energy were investigated at a fixed ion dose of $1 \times 10^{16} cm^{-2}$. After implantation, samples were oxidized in O_2 at 600°C for 5 hours. Implants at 100 keV

and 150 keV (R_p ≈ 790Å and 1200Å, respectively) resulted in non-uniform oxide growth with a banding similar to that which is observed when GaAs rapidly oxidizes. This effect is illustrated in the photomicrograph of Figure 17, which also shows the transition at the boundary between implanted and unimplanted regions.

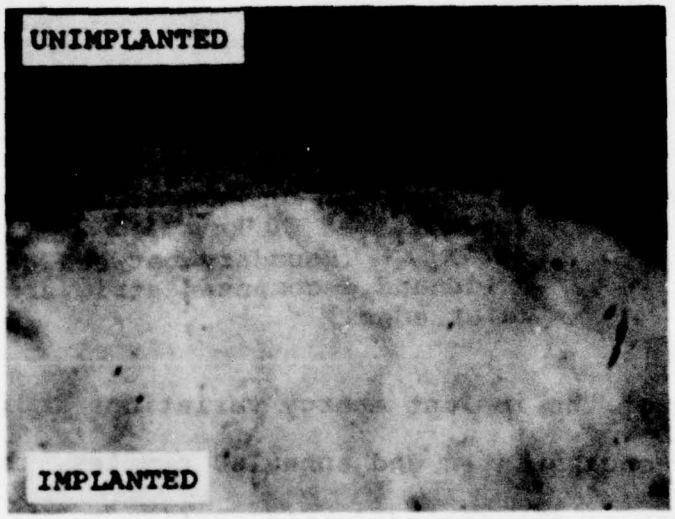


Figure 17. Oxide Growth on Unannealed Surface Implanted at 150 keV ($1 \times 10^{16} cm^{-2}$) (247X)

The low-energy implants at 30 keV and 60 keV (with R_p ≈ 250Å and 475Å, respectively) generally resulted in smooth oxides of uniform thickness. There was decomposition migrating inward from the wafer edges (Figure 18). This is believed to be due to the exposure of the unimplanted wafer edge during oxidation.

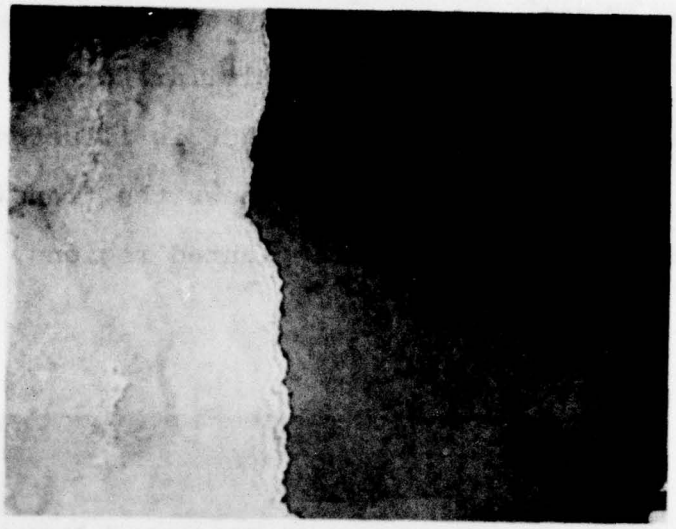


Figure 18. Oxide Growth on Unannealed Surface Implanted at 30 keV ($1 \times 10^{16} cm^{-2}$) (247X). (Boundary between uniform oxide and decomposed strip around wafer edge.)

The results of the implant energy variations indicate, as do those for the SiO_2-encapsulated and annealed samples, that the implant peak should be close to the semiconductor surface to avoid damage during oxidation. It may not necessarily be true that the lowest energy implants result in higher quality oxides. Comparison of higher dose ($3 \times 10^{16} cm^{-2}$) implants indicate a larger degree of structure and graininess in oxides grown on surfaces implanted at 30 keV than on those surfaces implanted at 60 keV. These effects are being investigated further.

Hot Implants--Oxide films which were grown on 'hot-implanted' samples were of a quality comparable to those grown on surfaces implanted at room temperature. No surface decomposition was visible

up to an implant temperature of 400°C. There was, however, a difference in oxide thickness noted between room temperature and hot implant samples which had received the same implant dose and oxidation temperature and time. For a phosphorus ion dose of $2 \times 10^{16} cm^{-2}$ and an oxidation time and temperature of 2.5 hours at 600°C in O_2 the the resulting film thicknesses were approximately 700Å and 1000Å for room temperature and 400°C implants, respectively. The reason for this difference is not known. If the high temperature implant results in less lattice damage, as expected, then a lower oxide growth rate would also be expected. Further experiments are planned to investigate this anomaly.

Ion Microprobe Analysis of Implant Profiles and Oxide Composition

Ion microprobe mass analysis (IMMA), fundamentally secondary ion mass spectrometry (SIMS) analysis of microarea regions, was used to examine the elemental depth composition of some of the ion implanted and oxidized surface layers. Depth profiles were obtained with an ARL IMMA using a primary beam of $^{18}O_2^+$ ions with a beam energy of 20 keV. Details of this analytical technique and its limitations are given in References 4 and 31.

Figures 19(a) and (b) show IMMA profiles for SiO_2-encapsulated/implanted samples before and after annealing, respectively. For comparison, an ideal LSS implant profile is included in Figure 19(a). This simplified ideal profile neglects third-moment effects, which can sometimes skew the profile about the implant peak (Reference 13).

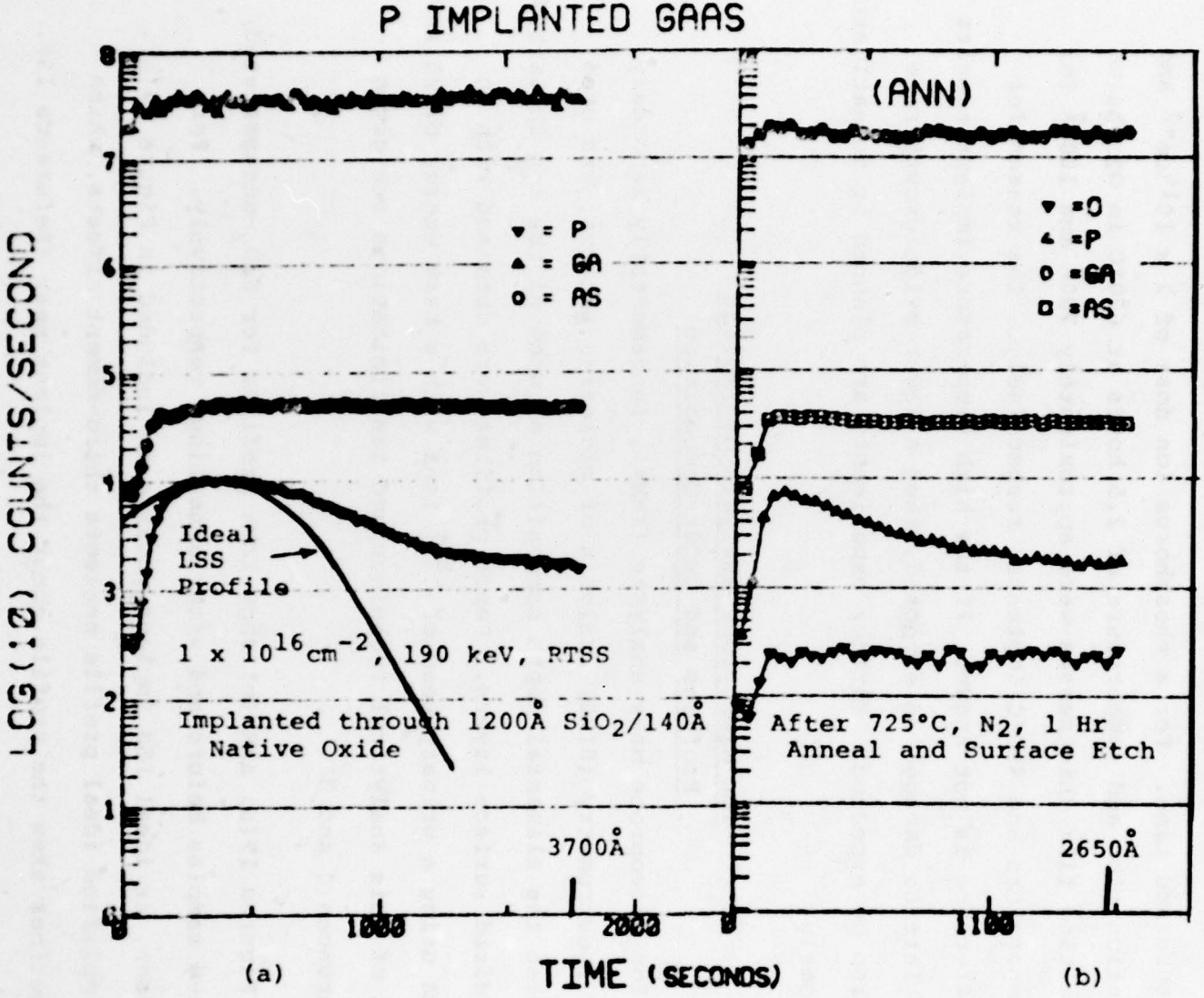


Figure 19. IMMA Profiles of Unannealed (a) and Annealed (b) Implanted Layers

The sample of Figure 19(b) had a 5 second surface etch to remove a slight residue. Although there is a slight sputter rate (therefore, ion yield) difference between the two samples in Figure 19(a) and (b), some comparisons can be made. There is apparently no significant diffusion of phosphorus into the substrate following annealing at 725°C. The phosphorus profile tails of both samples appear to extend somewhat deeper into the substrate than expected from LSS theory. It is believed that this is not necessarily enhanced diffusion during the implant, but rather a 'knock-in' effect which occurs when light mass elements are sputtered using a high energy beam (Ref. 31). With analytical techniques which use lower sputtering beam energies, such as the Auger and ESCA measurements planned later in this program, this 'knock-in' should be reduced to some extent.

The rapid increase in arsenic and phosphorus counts near the surface is another artifact of this technique, and is due to the establishment of equilibrium conditions during sputtering with the oxygen beam.

Figure 20 shows the profile of a sample which was implanted to a dose of $1 \times 10^{16} cm^{-2}$ at 140 keV with a substrate temperature of 300°C. A strict comparison cannot be made between Figures 19(a) and 20 because of the differing implant energies used; however, it appears that there is no significant phosphorus diffusion into the substrate as a result of the elevated temperature.

The elemental depth profile of an implanted and annealed sample, before and after oxidation at 600°C, is shown in Figures 21(a) and (b). The oxide profile indicates that there is apparently incorporation of phosphorus into the oxide in the region from the peak of the implant to the interface of the semiconductor. There is a deficiency of arsenic

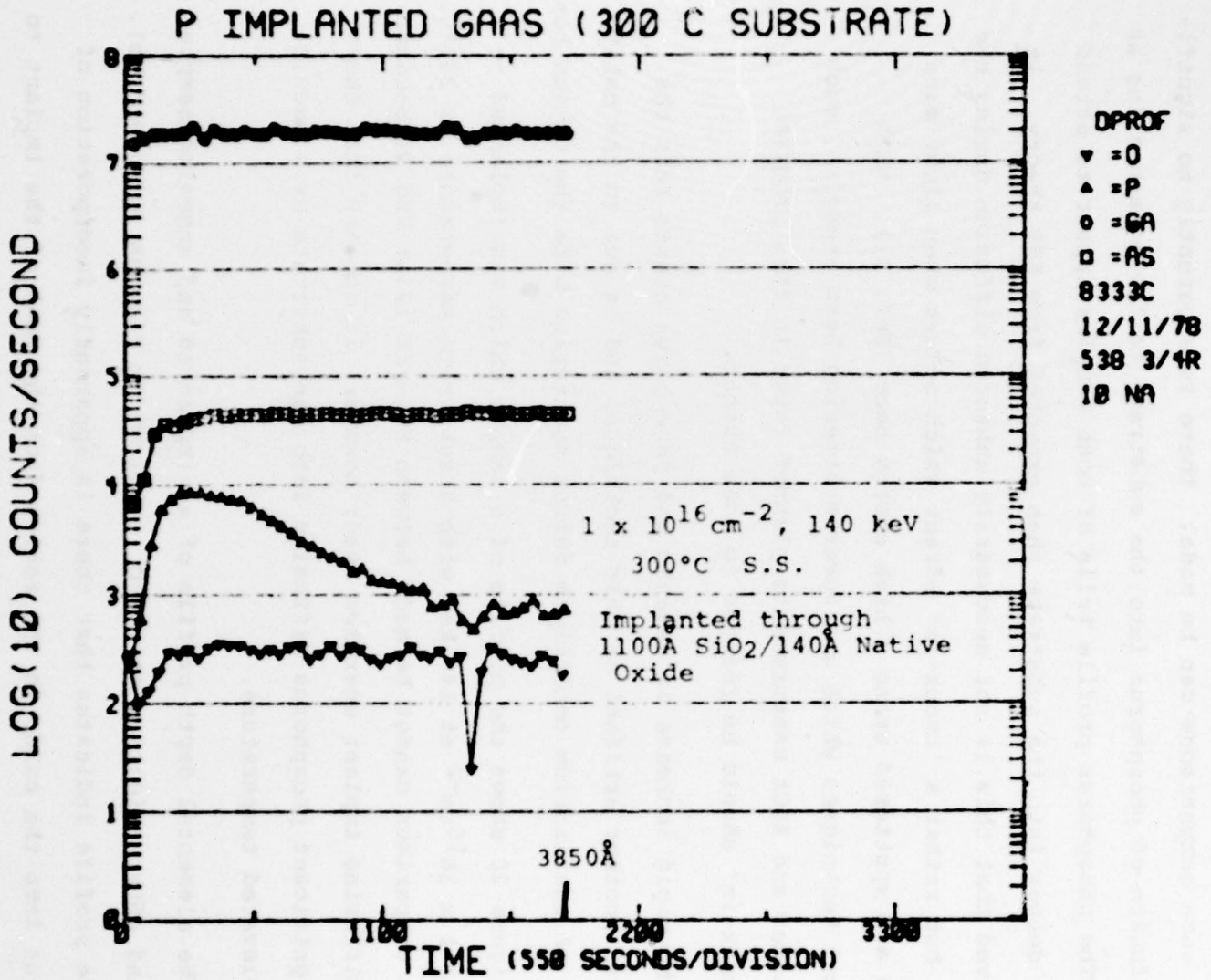


Figure 20. IMMA Profile of Sample Implanted at 300°C Substrate Temperature

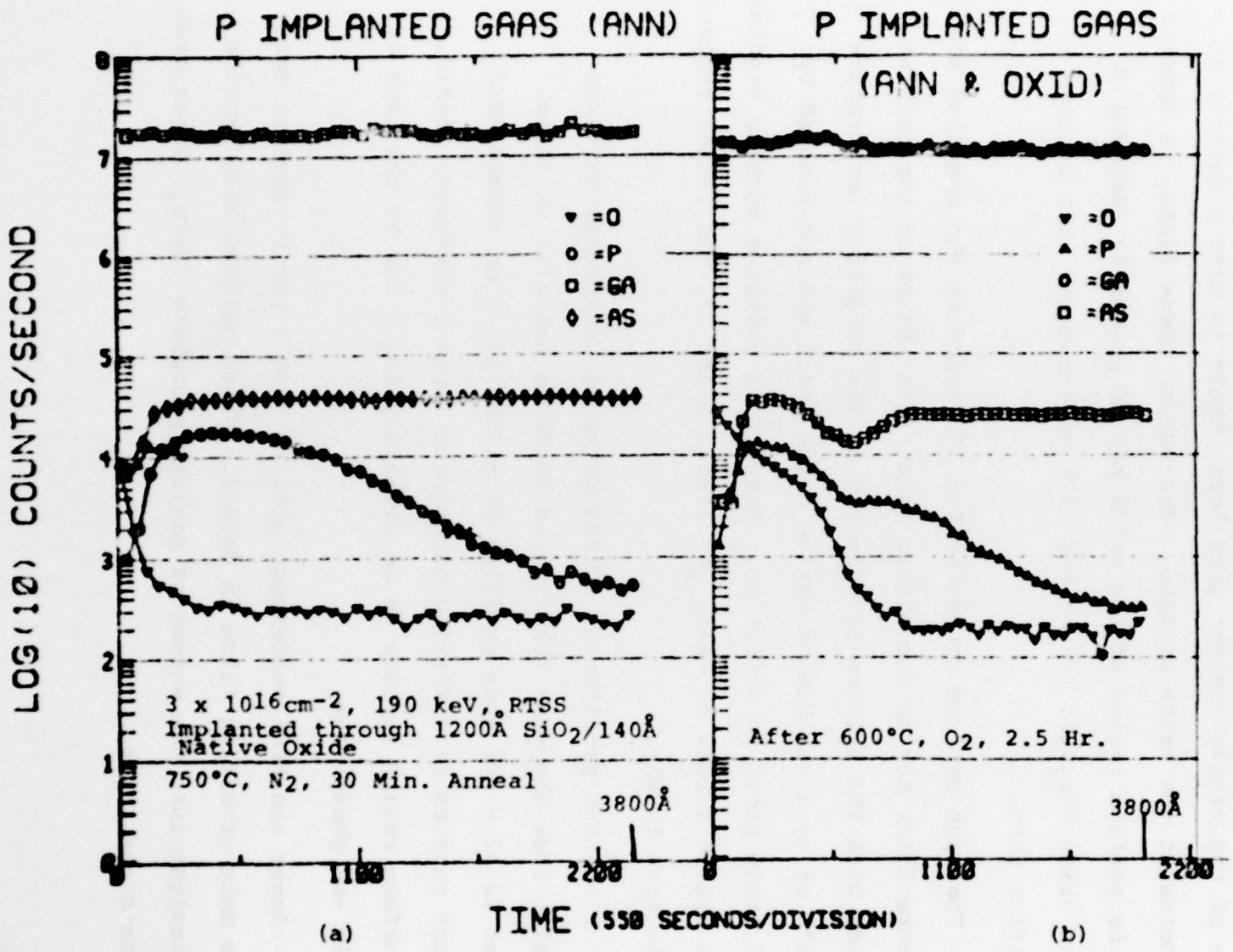


Figure 21. IMMA Profiles of Annealed (a) and Annealed/Oxidized (b) Implanted Layers

in the outer region of the oxide layer, which has been observed before in oxides on both GaAs and $GaAs_{1-x}P_x$. However, due to the nature of the single implant used here, there is also a deficit of phosphorus at the oxide surface. Because of these facts, it appears that the surface region of the oxide may be primarily composed of gallium oxide (Ga_2O_3). Auger and ESCA measurements will be used to to confirm this.

The high surface concentration of oxygen in the annealed sample of Figure 21(a) may be due either to an interaction of the gallium arsenide with the silicon dioxide cap at the annealing temperature of 725°C or to a residue of native oxide which was not removed by the HF strip prior to oxidation. Based upon previous etching studies on the native oxides on $GaAs_{1-x}P_x$ (Refs. 2 and 3), the latter explanation is more likely.

Elemental profiles of oxides grown on unannealed surfaces generally show the same features as those on annealed surfaces. Figures 22(a) - (c) show profiles of oxides grown on unimplanted GaAs and samples of differing phosphorus implant energies. Again, the surface region appears to be primarily Ga_2O_3 due to the lack of arsenic and phosphorus.

Auger and ESCA techniques will be used later to analyze some of the more promising films in detail. These methods will provide more insight into the extent of gallium phosphate ($GaPO_4$) incorporation into the oxide.

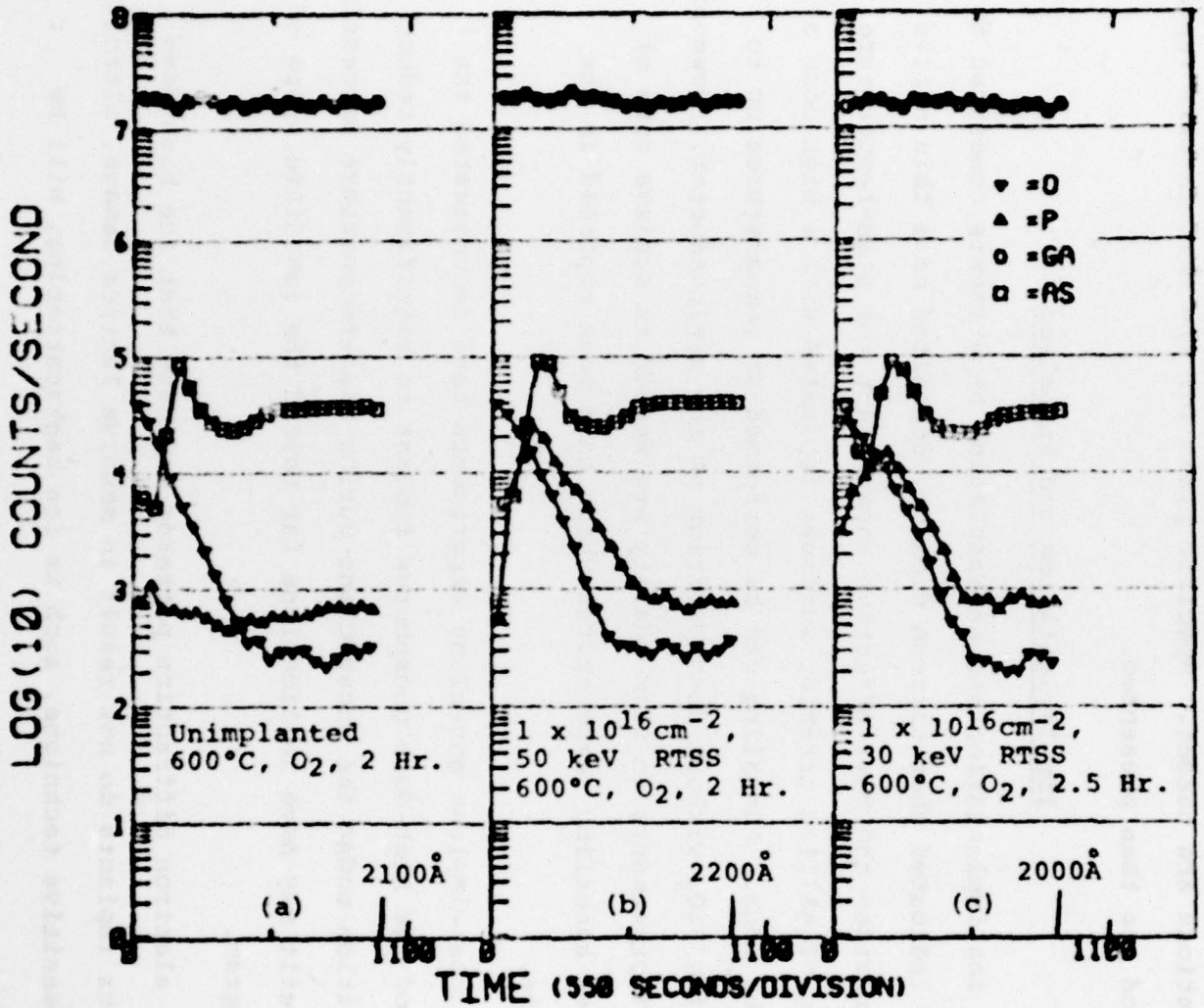


Figure 22. IMMA Profiles of Oxides Grown on Unimplanted(a) and Unannealed Implanted (b,c) Layers

SECTION IV

SUMMARY AND PLANS

This section summarizes some of the major results obtained during the initial phase of this program and discusses areas where further investigations are needed. Specific plans for the next interim reporting period are then presented.

Ion Implantation and Annealing

The ion implantation and encapsulation experiments conducted so far have indicated that silicon dioxide, deposited on a thin native oxide, provides the most effective encapsulant for high-temperature annealing of gallium arsenide surfaces implanted with a high dose of phosphorus ions. Annealing can be performed at temperatures up to 775°C using SiO_2 without decomposition of the semiconductor. However, further improvements in film quality are needed to achieve some of the higher annealing temperatures which have been reported in the literature.

The post-implant annealing experiments have demonstrated the ability of the high-dose phosphorus implant to significantly reduce decomposition under the encapsulant during high-temperature processing. This benefit may have implications far beyond the immediate scope of this program.

The electron diffraction patterns indicate that the high-dose phosphorus implants do not result in massive lattice damage, although a more sensitive technique, such as ion backscattering, will be

required to detect the defect levels which have been observed in earlier implants into GaAs.

Ion microprobe results indicate that there is no significant diffusion of phosphorus into the substrate during either post-implant annealing or hot substrate implantation. This indicates that the depth of the implanted region can be well controlled so that the advantageous properties of the underlying GaAs substrate can probably be utilized in the MIS devices to be fabricated in later phases of this program.

Oxidation

Oxides grown on the unannealed phosphorus-implanted surfaces have generally shown somewhat less decomposition and damage than those which were annealed with an encapsulant. The implant dose and energy variations attempted to date have narrowed the range of parameters for which acceptable oxides result. For unencapsulated surfaces it has been found that ions implanted at doses from 1 to 2 x $10^{16}cm^{-2}$ and energies from 30 keV to 60 keV result in oxides with the fewest visible defects. Encouragingly, these oxides are visually similar to those grown on $GaAs_{1-x}P_x$, and suggest that further improvements could lead to similar electrical properties. MIS capacitors will be fabricated on the most promising oxides which have been achieved recently and will be electrically characterized.

Additional experiments need to be performed using the higher implant doses ($\geq 1 \times 10^{17}cm^{-2}$) required to achieve the phosphorus mole fractions ($x \geq 0.3$) investigated in the previous oxidation work on single-crystal $GaAs_{1-x}P_x$. Oxidation should also be performed on surfaces with multiple implants tailored to result in a layer of uniform phosphorus concentration. This may minimize the formation

of Ga_2O_3 at the insulator surface, which apparently results due to low phosphorus content in the surface region following a single implant.

An oxidation temperature of 600°C has been used in the initial experiments. Lower oxidation temperatures should also be investigated to determine if arsenic loss from the insulator can be minimized. Earlier work has indicated that dielectric leakage currents are reduced when arsenic remains in the oxide. Different oxidation techniques, such as steam, high-pressure, or plasma, should be explored to find the most promising oxidation approach.

Plans for Next Reporting Period

During the next reporting period the implantation and oxidation experiments will continue. Post-implant annealing experiments using both silicon dioxide and silicon nitride will continue if improved film quality can be achieved. The effectiveness of these annealing procedures in removing lattice damage will continue to be assessed by electron diffraction and the electrical properties of subsequently oxidized surfaces. Other analytical techniques, such as ion back-scattering, will be used if available.

Oxidation of unannealed surfaces will continue, and additional implant parameter variations will be investigated. These variations include higher implant doses ($\geq 1 \times 10^{17} cm^{-2}$) and multiple implants. Implants at substrate temperatures greater than 400°C will also be performed if they can be scheduled on the new Rockwell MED GaAs implant facility, which is currently in the final checkout stages. In addition to these implant parameter investigations, experiments

are planned to examine alternate oxidation methods. These will include steam, high-pressure O_2 and steam, and plasma oxidation. These latter two techniques will utilize new equipment expected to be delivered during the next six months as part of an expansion of our GaAs device fabrication facilities.

More detailed analyses of the oxide composition will be carried out during the next period. Auger and ESCA techniques will be used to determine the composition of the most promising dielectrics. These results will be correlated with ion microprobe results on the same samples.

Detailed electrical characterization will begin on MIS capacitors fabricated on implanted and oxidized surfaces. Capacitance-voltage and current-voltage measurements will provide the primary means for evaluating the quality of these films. The results of this characterization will then be used to evaluate the most appropriate passivation insulator for application to the second phase of this program.

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